mailing receipt for the Preliminary Amendment are included with this response. Applicant respectfully requests that the claims added in that amendment be considered by the Examiner.

In this response, Claim 18 is amended to better define the scope of the claimed invention. New Claims 31 to 36 are added.

Claim 18 stands rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,589,412 to Iranmanesh, et al. Claim 18, as amended, includes the feature of "a substantially planar insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer, and said insulating layer having first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section, each said recess portion being immediately adjacent a respective said side surface of said third section." (See the paragraph in the instant specification bridging pages 10 and 11, as well as element 32 in Figure 1 of the instant specification for support for the amendment). Iranmanesh does not teach or suggest such a substantially planar insulating layer. Note for example that Iranmanesh's second oxide layer 118 is conformal rather than being substantially planar. Therefore, Applicant respectfully submits that Claim 18 is patentable over Iranmanesh.

Claims 19-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Iranmanesh in view of U.S. patent No. 5,360,757 to Lage. Applicant respectfully traverses the rejection. Claim 18 is nonobvious and patentable over Iranmanesh for the reasons presented above. Lage is cited by the Examiner for its teaching of a composite insulator layer comprising alternating layers of oxide and nitride. Lage does not cure the deficiencies of Iranmanesh. Therefore, Applicant respectfully submits that Claim 18 is patentable over Iranmanesh in view of Lage. Claims 19-22 (as well as newly added Claims 31 and 32) depend from Claim 18 and are therefore patentable

over the cited combination of references for at least the reasons presented above. With respect to Claim 20, note that that claim further defines the apparatus of Claim 19 wherein "said first and second portions of conductive material have respective upwardly facing third and fourth surface portions thereon, said third and fourth surface portions being substantially coplanar with a top surface of said insulator layer." Neither Iranmanesh nor Lage teach or suggest such a feature.

Claim 23, added in the aforementioned Preliminary Amendment, includes the feature wherein "top portions of said first and second terminals are substantially coplanar with said insulating layer covering said top portion of said control terminal." (See page 13 of the instant specification as well as Figures 4 and 5 for support for Claim 23). Neither Iranmanesh nor Lage teach or suggest such a feature. Therefore, Applicant submits that Claim 23 is nonobvious and patentable over those references. Claims 24-26 and new Claims 33 and 34 depend from Claim 23 and are therefore patentable over the cited references for at least the reasons presented above.

Claim 27, also added in the aforementioned Preliminary Amendment, includes the feature of "local interconnection terminals on opposing sides of said gate stack and abutting said insulating material on said side portions of said gate electrode, said local interconnection terminals extending above said plane of semiconductor material such that top portions of said local interconnection terminals are substantially coplanar with said insulating material covering said top portion of said gate electrode." (See page 13 of the instant specification as well as Figures 4 and 5 for support for Claim 27). Neither Iranmanesh nor Lage teach or suggest such a feature. Therefore, Applicant submits that Claim 27 is nonobvious and patentable over those references. Claims 28-30 and new Claims 35 and 36 depend from Claim 27 and are therefore patentable over the cited references for at least the reasons presented above.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 18-36. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Claims:

18. (amended) An apparatus comprising a semiconductor device which includes:

laterally spaced first and second sections with respective upwardly facing first and second surface portions thereon;

a third section projecting upwardly beyond each of said first and second surface portions from a location therebetween, said third section having two side surfaces on opposite sides thereof;

[an] a substantially planar insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer, and said insulating layer having first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section, each said recess portion being immediately adjacent a respective said side surface of said third section;

a first portion of conductive material disposed in said first recess portion; and

a second portion of conductive material disposed in said second recess portion.

Please add the following new claims:

31. The apparatus of Claim 18, wherein said side surfaces of said third section comprise an insulator, said insulator different from said substantially planar insulating layer.

32. The apparatus of Claim 31, wherein said insulator is nitride and said substantially planar insulating layer is oxide.

33. The apparatus of Claim 23, further comprising a substantially planar insulating layer coplanar with said insulating layer covering said top portion of said control terminal, wherein said control terminal and said first and second terminals are within an opening in said substantially planar insulating layer.

34. The apparatus of Claim 33, wherein said insulating layer covering said side portions and said top portion of said control terminal is nitride and said substantially planar insulating layer is oxide.

35. The integrated circuit of Claim 27, further comprising a substantially planar insulating layer coplanar with said insulating material covering said side and top portions of said gate stack, wherein said gate stack and said local interconnection terminals are within an opening in said substantially planar insulating layer.

36. The apparatus of Claim 35, wherein said insulating layer material covering said side and top portions of said gate stack is nitride and said substantially planar insulating layer is oxide.